

MJD340 (NPN) MJD350 (PNP)

High Voltage Power Transistors

DPAK For Surface Mount Applications

Designed for line operated audio output amplifier, switchmode power supply drivers and other switching applications.

Features

- Lead Formed for Surface Mount Applications in Plastic Sleeves (No Suffix)
- Electrically Similar to Popular MJE340 and MJE350
- 300 V (Min) – $V_{CEO(sus)}$
- 0.5 A Rated Collector Current
- Epoxy Meets UL 94 V-0 @ 0.125 in
- ESD Ratings: Human Body Model, 3B > 8000 V
Machine Model, C > 400 V
- These are Pb-Free Packages

MAXIMUM RATINGS

| Rating | Symbol | Max | Unit |
|---|----------------|---------------|--------------------------|
| Collector-Emitter Voltage | V_{CEO} | 300 | Vdc |
| Collector-Base Voltage | V_{CB} | 300 | Vdc |
| Emitter-Base Voltage | V_{EB} | 3 | Vdc |
| Collector Current – Continuous – Peak | I_C | 0.5 0.75 | Adc |
| Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above 25°C | P_D | 15 0.12 | W W/ $^\circ\text{C}$ |
| Total Power Dissipation (Note 1) @ $T_A = 25^\circ\text{C}$ Derate above 25°C | P_D | 1.56 0.012 | W W/ $^\circ\text{C}$ |
| Operating and Storage Junction Temperature Range | T_J, T_{stg} | -65 to +150 | $^\circ\text{C}$ |

THERMAL CHARACTERISTICS

| Characteristic | Symbol | Max | Unit |
|---|-----------------|------|---------------------------|
| Thermal Resistance, Junction-to-Case | $R_{\theta JC}$ | 8.33 | $^\circ\text{C}/\text{W}$ |
| Thermal Resistance, Junction-to-Ambient (Note 1) | $R_{\theta JA}$ | 80 | $^\circ\text{C}/\text{W}$ |
| Leading Temperature for Soldering Purpose | T_L | 260 | $^\circ\text{C}$ |

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

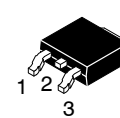
1. These ratings are applicable when surface mounted on the minimum pad sizes recommended.



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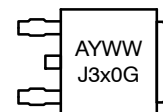
<http://onsemi.com>

**SILICON
POWER TRANSISTORS
0.5 AMPERE
300 VOLTS, 15 WATTS**



**DPAK
CASE 369C
STYLE 1**

MARKING DIAGRAM



A = Assembly Location
Y = Year
WW = Work Week
J3x0 = Device Code
x = 4 or 5
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

| Characteristic | Symbol | Min | Max | Unit |
|----------------|--------|-----|-----|------|
|----------------|--------|-----|-----|------|

OFF CHARACTERISTICS

| | | | | |
|--|----------------|-----|-----|----|
| Collector-Emitter Sustaining Voltage (Note 2) ($I_C = 1\text{ mA}$, $I_B = 0$) | $V_{CEO(sus)}$ | 300 | - | V |
| Collector Cutoff Current ($V_{CB} = 300\text{ V}$, $I_E = 0$) | I_{CEO} | - | 0.1 | mA |
| Emitter Cutoff Current ($V_{BE} = 3\text{ V}$, $I_C = 0$) | I_{EBO} | - | 0.1 | mA |

ON CHARACTERISTICS (Note 2)

| | | | | |
|--|---------------|----|-----|---|
| DC Current Gain ($I_C = 50\text{ mA}$, $V_{CE} = 10\text{ V}$) | h_{FE} | 30 | 240 | - |
| Collector-Emitter Saturation Voltage ($I_C = 100\text{ mA}$, $I_B = 10\text{ mA}$) | $V_{CE(sat)}$ | - | 1 | V |
| Base-Emitter On Voltage ($I_C = 1\text{ A}$, $V_{CE} = 10\text{ V}$) | $V_{BE(on)}$ | - | 1.5 | V |

DYNAMIC CHARACTERISTICS

| | | | | |
|---|-------|----|---|-----|
| Current Gain — Bandwidth Product ($I_C = 50\text{ mA}$, $V_{CE} = 10\text{ V}$, $f = 10\text{ MHz}$) | f_T | 10 | - | MHz |
|---|-------|----|---|-----|

2. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.

TYPICAL CHARACTERISTICS

MJD340

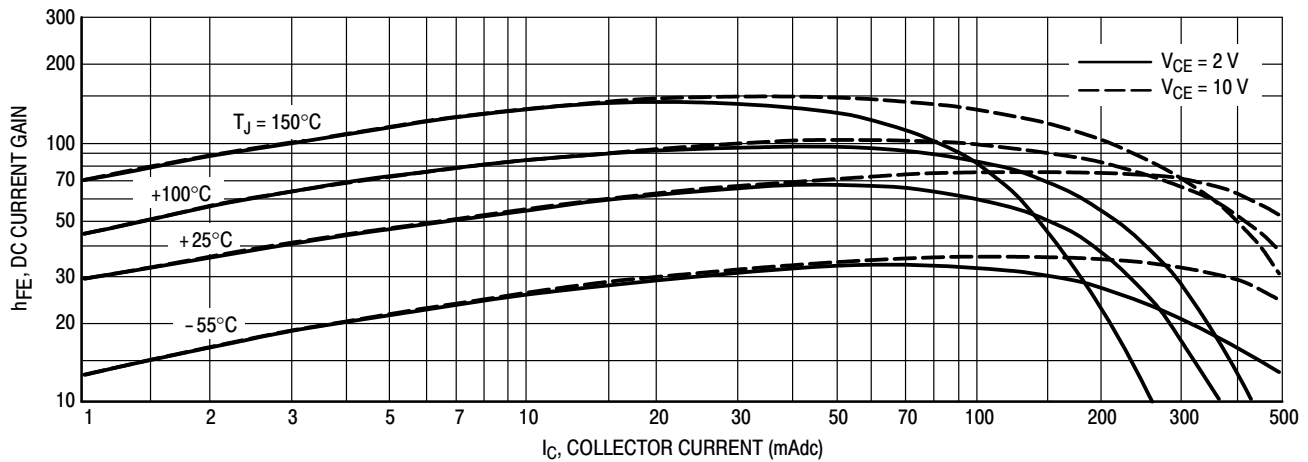


Figure 1. DC Current Gain

MJD340 (NPN) MJD350 (PNP)

MJD340

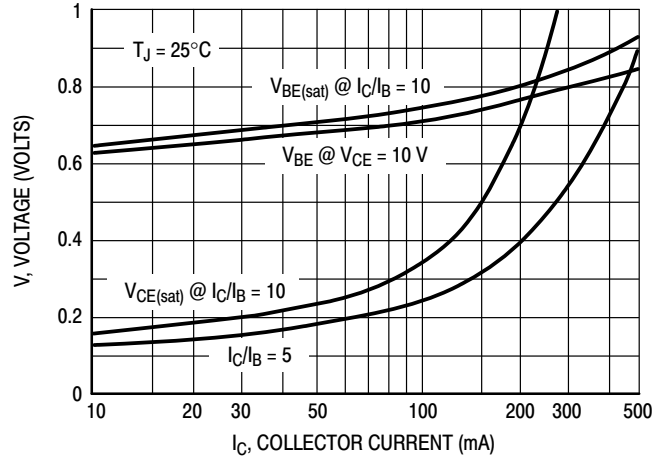


Figure 2. "On" Voltages

MJD350

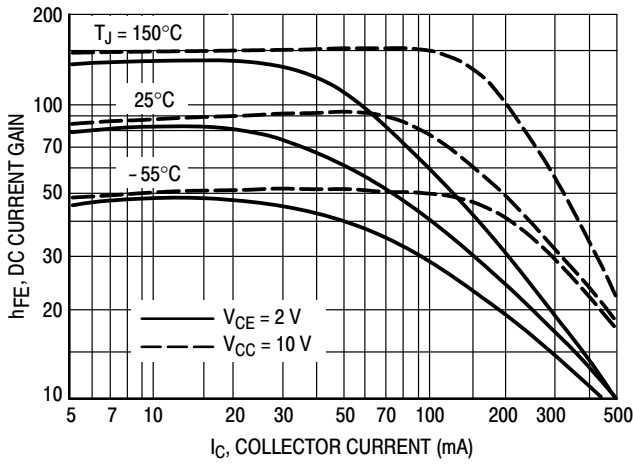


Figure 3. DC Current Gain

MJD350

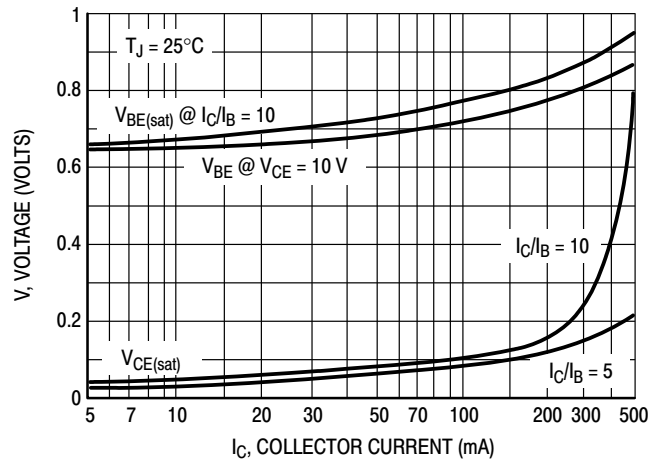


Figure 4. "On" Voltages

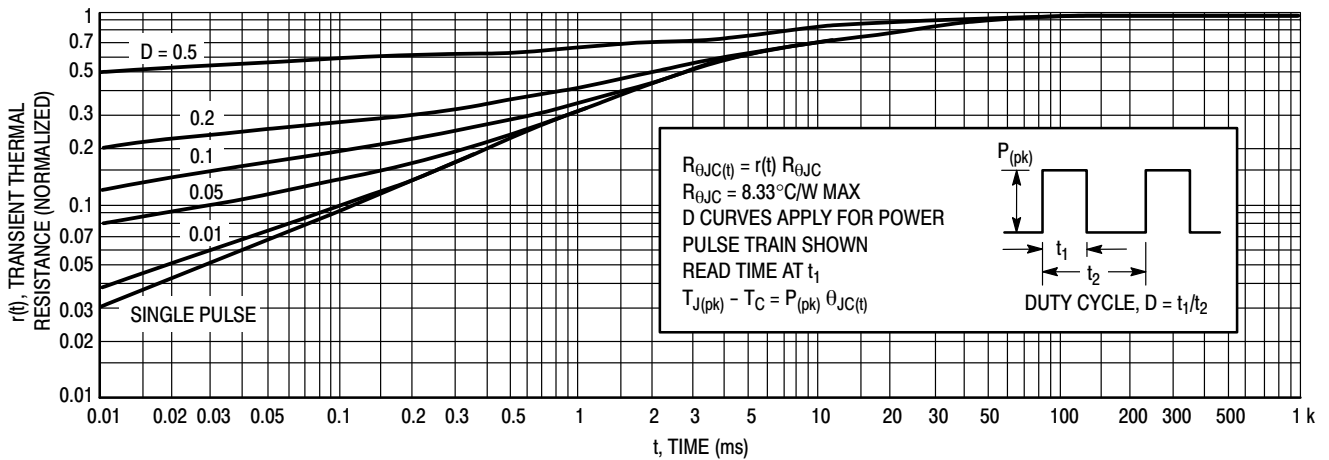


Figure 5. Thermal Response

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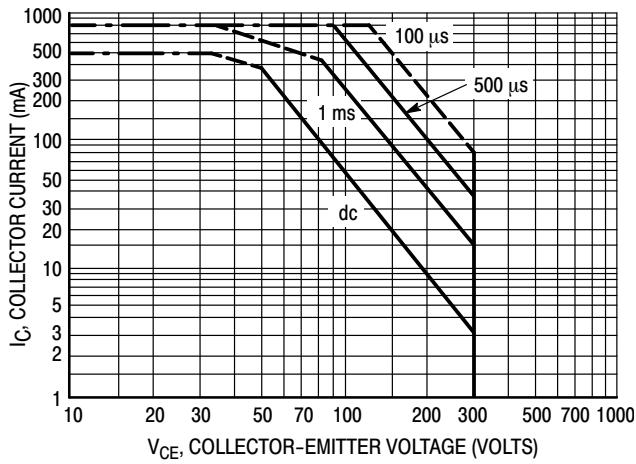


Figure 6. Active Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 6 is based on $T_{J(pk)} = 150^\circ\text{C}$; T_C is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided $T_{J(pk)} \leq 150^\circ\text{C}$. $T_{J(pk)}$ may be calculated from the data in Figure 5. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

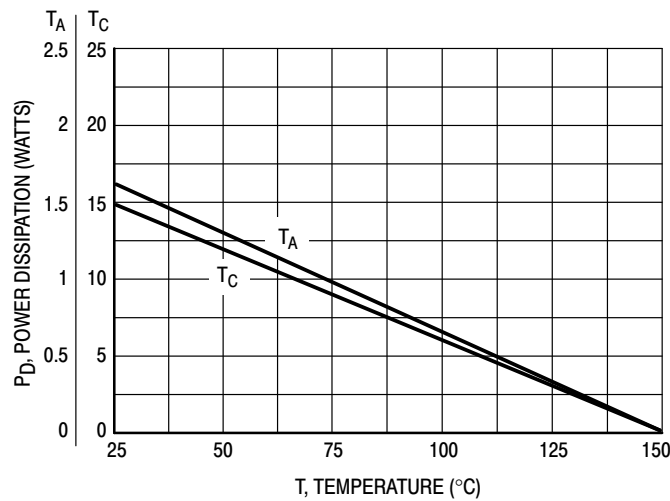


Figure 7. Power Derating

ORDERING INFORMATION

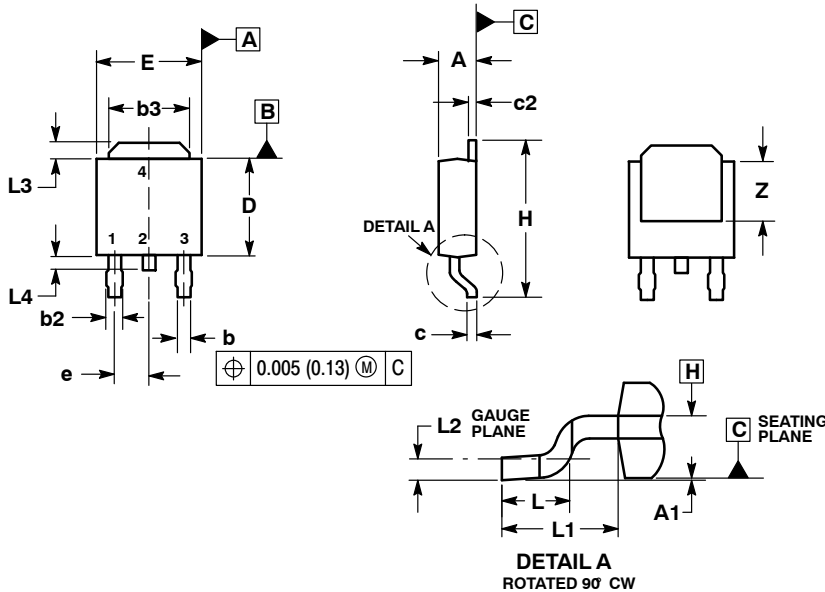
| Device | Package | Shipping [†] |
|-----------|-------------------|-----------------------|
| MJD340G | DPAK (Pb-Free) | 75 Units / Rail |
| MJD340RLG | DPAK (Pb-Free) | 1800 / Tape & Reel |
| MJD340T4G | DPAK (Pb-Free) | 2500 / Tape & Reel |
| MJD350G | DPAK (Pb-Free) | 75 Units / Rail |
| MJD350T4G | DPAK (Pb-Free) | 2500 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

DPAK CASE 369C-01 ISSUE D

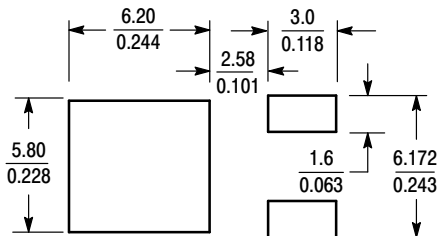


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

| DIM | INCHES | | MILLIMETERS | |
|-----|-----------|-------|-------------|-------|
| | MIN | MAX | MIN | MAX |
| A | 0.086 | 0.094 | 2.18 | 2.38 |
| A1 | 0.000 | 0.005 | 0.00 | 0.13 |
| b | 0.025 | 0.035 | 0.63 | 0.89 |
| b2 | 0.030 | 0.045 | 0.76 | 1.14 |
| b3 | 0.180 | 0.215 | 4.57 | 5.46 |
| c | 0.018 | 0.024 | 0.46 | 0.61 |
| c2 | 0.018 | 0.024 | 0.46 | 0.61 |
| D | 0.235 | 0.245 | 5.97 | 6.22 |
| E | 0.250 | 0.265 | 6.35 | 6.73 |
| e | 0.090 BSC | | 2.29 BSC | |
| H | 0.370 | 0.410 | 9.40 | 10.41 |
| L | 0.055 | 0.070 | 1.40 | 1.78 |
| L1 | 0.108 REF | | 2.74 REF | |
| L2 | 0.020 BSC | | 0.51 BSC | |
| L3 | 0.035 | 0.050 | 0.89 | 1.27 |
| L4 | --- | 0.040 | --- | 1.01 |
| Z | 0.155 | --- | 3.93 | --- |

SOLDERING FOOTPRINT*



SCALE 3:1 (mm/inches)

STYLE 1:

- PIN 1. BASE
- COLLECTOR
- EMITTER
- COLLECTOR

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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